Remarks

Applicants respectfully request reconsideration of this application as amended. Claims 1, 3, 5, 6, 8, 11-14, 20, 22 and 24 have been amended. No claims have been cancelled. Therefore, claims 1-24 are presented for examination.

In the Office Action, claims 8-10 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards the invention. Particularly, claim 8 has been rejected due to an informality. Applicants submit that claim 8 has been amended to appear in proper condition for allowance.

Claims 1-4, 6-8, 11-12, 14-16 and 20-23 stand rejected under 35 U.S.C. §102(e) as being anticipated by Tischler (U.S. Patent No. 6,483,516) ("Tischler"). Applicants submit that the present claims are patentable over Tischler.

Tischler discloses a multimedia processor 134 including a central processing unit (CPU) 136, a graphics unit 138, a shared L2 cache 140, a four port bus interface unit 142, a memory controller 144 and a I/O interface unit 146. The bus interface unit 142 couples together the CPU 136, the graphics unit 138, the L2 cache 140, the memory controller 144 and the I/O interface unit 146. The CPU 136 shares a single bus with the L2 cache 140 to the bus interface unit (BIU) 142. See Tischler at Figure 3 and col. 4, ll. 47-64. The graphics unit 138 includes an arbitration and interface unit 154, a video controller unit 155, a display controller unit 158, a VGA unit 160 and a 2D/3D graphics pipeline unit 162 with an L1 texture cache 164. The 2D/3D graphics pipeline unit 162 generates 2D and 3D graphics data and includes a dedicated setup unit (not specifically shown) along with a rasterization unit (also not specifically shown) and a first level (i.e. L1) texture cache 164 as part of a hierarchical texture cache discussed in detail herein below (Figure 4 and col. 5, ll. 28 – col. 6, ll. 13).

Claim 1 recites a graphics core to compute graphical transformations via supersampling techniques. Applicants submit that there is no disclosure in Tischler of using

supersampling as an anti-aliasing technique. Tischler discloses in the background that displaying 3D graphics is typically characterized by a pipelined process having tessellation, geometry and rendering stages. The tessellation stage is responsible for decomposing an object into polygons for simplified processing while the geometry stage is responsible for transforming the tessellated object. The rendering stage rasterizes the polygons into pixels and applies visual effects such as texture mapping, MIP mapping, Z buffering, depth cueing, anti-aliasing and fogging. However, there is no disclosure of using supersampling techniques. Therefore, claim 1 is patentable over Tischler.

Claims 2-10 depend from claim 1 and include additional limitations. Accordingly, claims 2-10 are also patentable over Tischler.

Claim 11 recites amplifying polygons at a graphics core and rendering the polygons into a unified graphics cache. Applicants submit that Tischler does not disclose amplifying polygons at a graphics core. Thus, claim 11 is also patentable over Tischler. Because claims 12-19 depend from claim 11 and include additional limitations, claims 12-19 are also patentable over Tischler.

Claim 20 recites a graphics accelerator to compute graphical transformations via supersampling techniques. Thus, for the reasons stated above with respect to claim 1, claim 20 is also patentable over Tischler. Since claims 21-24 depend from claim 11 and include additional limitations, claims 21-24 are also patentable over Tischler.

Claims 5, 19 and 24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Tischler in view of Penna et al. (U.S. Patent No. 6,498,606) ("Penna"). Applicants submit that the present claims are patentable over Tischler even in view of Penna.

Penna discloses an image processing system for providing two-dimensional pixel images. The system includes a plurality of polygonal image primitives and a background. The polygonal image primitives represent a three-dimensional object, a Z buffer and a color buffer that are cleared by the steps of rendering image primitives relating to foreground in the color buffer (354) and the Z buffer (353); and subsequently scanning the Z buffer and for

each pixel, if the Z value is a predetermined background value such as zero (357), clearing the corresponding location in the color buffer to background color (358), and if the Z value is not the predetermined background value, clearing the Z buffer to that predetermined background value (359). In the method, either a Z buffer or a color value is written during the buffer clearing process, but never both. The pixels may be read from cache in groups, the size of a group being selected to maximize the possibility of all consecutive pixels in a group being either foreground or background pixels. Further bandwidth saving may be achieved by the use of a tile buffer and two output buffers. See Penna at Abstract.

Nevertheless, Penna does not disclose or suggest computing graphical transformations via supersampling techniques or amplifying polygons at a graphics core and rendering the polygons into a unified graphics cache. As described above, Tischler does not disclose or suggest such limitations. Consequently, any combination of Penna and Tischler would also not disclose the limitations. Therefore, the present claims are patentable over Tischler in view of Penna.

Claims 9, 13 and 17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Tischler in view of Pfister et al. (U.S. Patent No. 6,448,968) ("Pfister"). Applicants submit that the present claims are patentable over Tischler even in view of Pfister.

Pfister discloses a method for modeling a representation of a graphic object. A surface of the object is partitioned into a plurality of cells having a grid resolution related to an image plane resolution. A single zero-dimensional surface element is stored in the memory for each cell located on the surface of the object. The surface elements in adjacent cells are connected by links, and attributes of the portion of the object contained in the cell are assigned to each surface element and each link. The location of the attributed surface elements can be moved according to forces acting on the object. See Pfister at Abstract.

However, Pfister does not disclose or suggest computing graphical transformations via supersampling techniques or amplifying polygons at a graphics core and rendering the polygons into a unified graphics cache. Accordingly, any combination of Penna and Pfister

would also not disclose the limitations. Thus, the present claims are patentable over Tischler in view of Pfister.

Claims 10 and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tischler in view of Pfister et al. as applied to claims 1-9 and 11-17 above, in further in view of Li et al, (U.S. Patent No. 5,860,060) ("Li"). Applicants submit that the present claims are patentable over Tischler and Pfister even in view of Li.

Li discloses a data processing device that uses a portion of random access memory 121 as an output buffer 124 for holding a portion of a stream of PCM data which is to be output to a digital to analog converter 530. D/A 530 forms a left analog channel and a right analog channel for speaker subsystems 814 and 815. The PCM data stream is stored in the output buffer so that PCM data samples which pertain to the left channel are stored at even address and PCM data samples which pertain to the right channel are stored at odd address. Control circuitry 145 monitors direct memory access (DMA) transfers which transfer PCM data samples to PCM serializer 142. By comparing the address of each DMA transfer to a left/right channel signal from the D/A, the control circuitry can verify that channel synchronization is correct. If a synchronization error is detected, an channel synchronization error correction procedure is invoked. See Li at Abstract.

Nonetheless, Li does not disclose or suggest computing graphical transformations via supersampling techniques or amplifying polygons at a graphics core and rendering the polygons into a unified graphics cache. As discussed above, neither Tischler nor Pfister disclose or suggest computing graphical transformations via supersampling techniques or amplifying polygons at a graphics core and rendering the polygons into a unified graphics cache. Therefore, any combination of Tischler, Pfister and Li would also not disclose such limitations. Thus, the present claims are patentable over Tischler in view of Pfister and Li.

Applicants respectfully submit that the rejections have been overcome, and that the claims as amended are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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Date: April 16, 2003

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